Amendments the Specification:

Please replace paragraph **[0028]** beginning on pages 14-15 with the following amended paragraph **[0028]**:

[0028] FIG. 2 is a simplified schematic diagram of a portion of a feedback circuit 200 of the regulator device 100 employing margin control according to an exemplary embodiment of the present invention. Similar components from FIG. 1 assume identical reference numbers. The current mirror 115 has a pair of current output terminals coupled across a resistor RMU/D for generating the up margining voltage VMARG UP. The current mirror 117 has a pair of current output terminals coupled across a resistor RMD/D for generating the down margining voltage VMARG DOWN. The current from the current mirror 117 is shown reversed through the resistor RMD/D to effectively generate the down margining voltage as -VMARG DOWN. VMARG UP is provided to a selectable terminal A and -VMARG DOWN is provided to a selectable terminal B of a SPDT switch SW3, having a common pole coupled to a selected margining voltage VMARG. The switch SW3 is controlled by the MARCTRL pin ~~105~~ 103 (or signal MARCTRL or version thereof), so that VMARG UP is selected as VMARG when MARCTRL is high and -VMARG DOWN is selected as VMARG when MARCTRL is low. The VMARG signal is applied to one input of a two-input combiner or adder 201, which receives VREF at its other input. The adder 201 adds VREF and VMARG together to generate a reference voltage with margin signal VRM. The VRM signal is provided to the input of an operational transconductance amplifier (OTA) circuit 203, which has an output that generates a set point voltage VSP used to control the output voltage level of the regulator device 100. The output of the OTA circuit 203 is coupled to one end of a soft-start capacitor CSS and to the non-inverting input of an error amplifier (EA) 205. In the embodiment shown, the capacitor CSS is implemented off-chip and coupled through a pin 207. The EA 205 receives a feedback voltage signal VFB at its inverting input, and generates a compensation signal COMP at its output.